UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/524,535	02/10/2005	Jeroen Anton Johan Leijten	NL02 0751 US	1509

24738 7590 05/17/2007

PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
INTELLECTUAL PROPERTY & STANDARDS
1109 MCKAY DRIVE, M/S-41SJ
SAN JOSE, CA 95131

EXAMINER	
TREAT, WILLIAM M	
ART UNIT	**PAPER NUMBER**
2181	

MAIL DATE	DELIVERY MODE
05/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/524,535	LEIJTEN, JEROEN ANTON JOHAN	
	Examiner	Art Unit	
	William M. Treat	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 March 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-11 are presented for examination.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pechanek et al. (Patent No. 6,101,592) in view of Pechanek et al. (Patent No. 6,173,389) incorporated by reference in Pechanek '592.

4. Pechanek '592 taught the invention of exemplary claim 1, in substance, including a processing apparatus, comprising: an input means for inputting data (157); a register file for storing said input data (PE Config. Register File); at least a first and a second issue slot, wherein each issue slot comprises a functional unit (col. 14, lines 41-46); and wherein the processing apparatus is conceived for processing data retrieved from the register file based on control signals generated from a set of instructions being executed in parallel (col. 6, lines 39-51), the set of instructions comprising at least a first and a second instruction (Fig. 1B), the first issue slot being controlled by a first control word corresponding to the first instruction and the second issue slot being controlled by a second control word corresponding to the second instruction (col. 14, lines 41-46), characterized in that the width of the first control word is different from the width of the second control word (16B).

5. Pechanek '592 did not teach "wherein each issue slot comprises a plurality of functional units". However, Pechanek '389 taught the Pechanek '592 system has the

functionality for one instruction (i.e., one issue slot) to access all of the functional units (Fig. 5, element 535, col. 7, lines 40-45). Given Pechanek '592s teaching that "For example, the execution units 131 in the combined SP/PEO can be separated into a set of execution units optimized for the control function, e.g. fixed point execution units, and the PE0 as well as the other PEs can be optimized for a floating point application", one of ordinary skill in the art would be motivated to use the concept of multiple execution units per slot so that successive VLIW instructions which each had a sub-instruction destined for the same non-pipelined, multi-cycle execution unit would not find would not find one or more of the successive VLIW instructions blocked from execution by having to await the completion of one multi-cycle FP instruction in the slot for the one non-pipelined, multi-cycle execution unit. Also, the examiner takes Official Notice of the fact that VLIW processors with more than one execution unit per slot were known at the time of applicant's invention which chose to assign dissimilar execution units to instruction slots in order to have a wide variety of execution unit types while still economizing on busses, chip real estate, etc.

6. As to claim 2, Pechanek '592 taught an apparatus according to Claim 1, wherein said processing apparatus is a VLIW processor and wherein said set of instructions is grouped in a VLIW instruction (Abstract).

7. As to claim 3, Pechanek '592 taught an apparatus according to Claim 2, wherein the VLIW instruction is a compressed VLIW instruction, comprising dedicated bits for encoding of NOP operations (If either compacted instruction is a 15-bit NOP then based

upon the type of NOP (bit 7 FIG. 3B) then execute the two compacted instructions sequentially or in parallel". – col. 16, lines 21-25).

8. As to claim 4, Pechanek '592 taught an apparatus according to Claim 3, comprising a decompression means for decompressing the compressed VLIW instruction and wherein the decompression means is conceived to derive information on the control word width using the dedicated bits (col. 4, line 53 through col. 5, line 63 and col. 6, lines 39-42).

9. As to claim 5, Pechanek '592 taught an apparatus according to Claim 1, which further comprises a connection network for coupling the register file and the issue slots (157).

10. As to claim 6, Pechanek '592 taught an apparatus according to Claim 2, wherein the register file is a distributed register file (Fig. 1A, PE Config. Register File in each PE).

11. As to claim 7, Pechanek '592 taught an apparatus according to Claim 1, wherein the width of the first and the second control word is an integer multiple of a predetermined value (Fig. 1B, element 16B).

12. As to claims 8-11, they fail to teach or define over rejected claims 1-7.

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

14. Kawaguchi (Patent No. 6,360,312) depicted a prior art VLIW processor in his Fig. 1 having multiple execution/functional units per slot and discussed the processor in his Background of the Invention section.

15. Applicant's arguments filed 3/27/2007 have been fully considered but they are not persuasive.

16. Applicants have argued, in substance, (a) there is no teaching or motivation recited in Pechanek to support providing multiple execution/functional units per slot and (b) there is no teaching in Pechanek of compressed VLIW instructions with dedicated bits for encoding NOP operations as well as circuitry to decompress.

17. As to 16(a), the case law applicant cited has been superseded by a recent Supreme Court decision (*KSR Int'l Co. v. Teleflex, Inc.*, No. 04-1350 (U.S. Apr. 30, 2007)). As to a more detailed explanation of the examiner's position, see paragraph 5, *supra*.

18. As to 16(b), applicant should review paragraph 7, *supra*. The examiner would also point out that he considers circuitry/means for Pechanek '592 to be inherent or the instructions would be worthless in Pechanek's system.

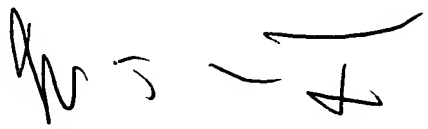
19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

20. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

21. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175.

22. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



WILLIAM M. TREAT
PRIMARY EXAMINER